



STQ3NK50ZR-AP STD3NK50Z - STD3NK50Z-1

N-CHANNEL 500V - 2.8Ω - 2.3A TO-92/DPAK/IPAK
Zener-Protected SuperMESH™ MOSFET

Table 1: General Features

TYPE	V _{DSS}	R _{DS(on)}	I _D	P _w
STQ3NK50ZR-AP	500 V	3.3 Ω	0.5 A	3 W
STD3NK50Z	500 V	3.3 Ω	2.3 A	45 W
STD3NK50Z-1	500 V	3.3 Ω	2.3 A	45 W

- TYPICAL R_{DS(on)} = 2.8Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- ESD IMPROVED CAPABILITY
- 100% AVALANCHE TESTED
- NEW HIGH VOLTAGE BENCHMARK
- GATE CHARGE MINIMIZED

DESCRIPTION

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding application. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products

APPLICATIONS

- AC ADAPTORS AND BATTERY CHARGERS
- SWITCH MODE POWER SUPPLIES (SMPS)
- LIGHTING

Figure 1: Package

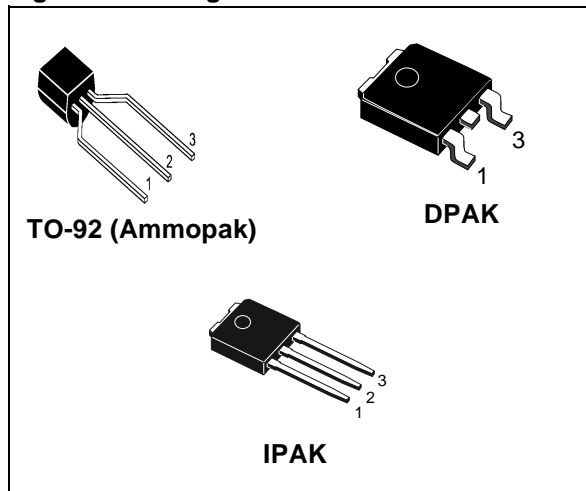


Figure 2: Internal Schematic Diagram

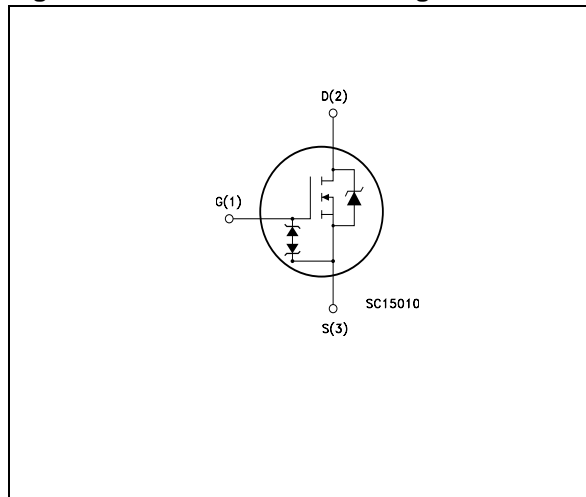


Table 2: Order Coder

SALES TYPE	MARKING	PACKAGE	PACKAGING
STQ3NK50ZR-AP	Q3NK50ZR	TO-92	AMMOPAK
STD3NK50Z	D3NK50Z	DPAK	TAPE & REEL
STD3NK50Z-1	D3NK50Z	IPAK	TUBE

Table 3: Absolute Maximum ratings

Symbol	Parameter	Value		Unit
		DPAK/IPAK	TO-92	
V _{DS}	Drain-source Voltage (V _{GS} = 0)	500		V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	500		V
V _{GS}	Gate- source Voltage	±30		V
I _D	Drain Current (continuous) at T _C = 25°C	2.3	0.5	A
I _D	Drain Current (continuous) at T _C = 100°C	1.45	0.32	A
I _{DM} (•)	Drain Current (pulsed)	9.2	2	A
P _{TOT}	Total Dissipation at T _C = 25°C	45	3	W
	Derating Factor	0.36	0.025	W/°C
V _{ESD(G-S)}	Gate source ESD (HBM-C=100 pF, R= 1.5KΩ)	2000		V
dv/dt (1)	Peak Diode Recovery voltage slope	4.5		V/ns
T _j T _{stg}	Operating Junction Temperature Storage Temperature	-55 to 150		°C

(•) Pulse width limited by safe operating area

(1) I_D ≤ 2 di/dt ≤ 200A/μs, V_{DD} ≤ V_{(BR)DSS}

Table 4: Thermal Data

		DPAK	IPAK	TO-92	Unit
R _{thj-case}	Thermal Resistance Junction-case Max	2.77		--	°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient Max	50 (#)	100	120	°C/W
R _{thj-lead}	Thermal Resistance Junction-lead Max	--	--	40	°C/W
T _l	Maximum Lead Temperature For Soldering Purpose	275		260	°C

(#) When mounted on 1inch² FR4, 2 Oz copper board.

Table 5: Avalanche Characteristics

Symbol	Parameter	Max. Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repertitive (pulse width limited by T _j max)	2.3	A
E _{AS}	Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	120	mJ

Table 6: GATE-SOURCE ZENER DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV _{GSO}	Gate-Source Breakdown Voltage	I _{gs} =± 1mA (Open Drain)	30			V

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in-back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

ELECTRICAL CHARACTERISTICS ($T_{CASE} = 25^{\circ}C$ UNLESS OTHERWISE SPECIFIED)

Table 7: On/Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 1\text{ mA}, V_{GS} = 0$	500			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}, T_C = 125^{\circ}C$			1 50	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 20V$			± 10	μA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 50\ \mu A$	3	3.75	4.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10V, I_D = 1.15\text{ A}$		2.8	3.3	Ω

Table 8: Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (1)$	Forward Transconductance	$V_{DS} = 15\text{ V}, I_D = 1.15\text{ A}$		1.5		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25V, f = 1\text{ MHz}, V_{GS} = 0$		280 42 8		pF pF pF
$C_{oss\ eq. (3)}$	Equivalent Output Capacitance	$V_{GS} = 0V, V_{DS} = 0V\text{ to }400\text{ V}$		27.5		pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on Delay Time Rise Time Turn-off Delay Time Fall Time	$V_{DD} = 250\text{ V}, I_D = 1.15\text{ A}$ $R_G = 4.7\ \Omega, V_{GS} = 10\text{ V}$ (see Figure 19)		8 13 24 14		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 400\text{ V}, I_D = 2.3\text{ A},$ $V_{GS} = 10V$ (see Figure 22)		11 2.5 5.6	15	nC nC nC

Table 9: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM} (2)$	Source-drain Current Source-drain Current (pulsed)				2.3 9.2	A A
$V_{SD} (1)$	Forward On Voltage	$I_{SD} = 2.3\text{ A}, V_{GS} = 0$			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 2.3\text{ A}, di/dt = 100\text{ A}/\mu s$ $V_{DD} = 40V, T_j = 25^{\circ}C$ (see Figure 20)		250 745 6		ns μC A
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 2.3A, di/dt = 100\text{ A}/\mu s$ $V_{DD} = 40V, T_j = 150^{\circ}C$ (see Figure 20)		300 960 6.2		ns μC A

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

2. Pulse width limited by safe operating area.

3. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Figure 3: Safe Operating Area For TO-92

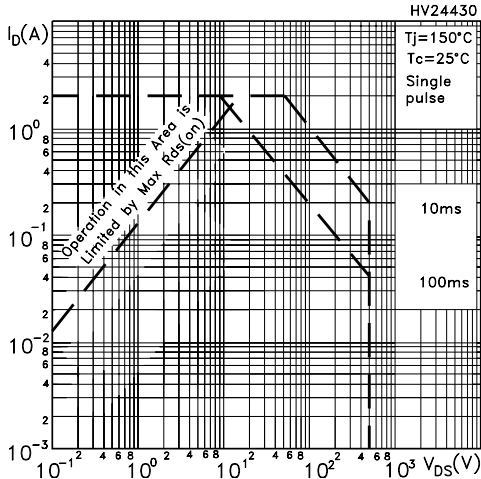


Figure 4: Safe Operating Area For DPAK / IPAK

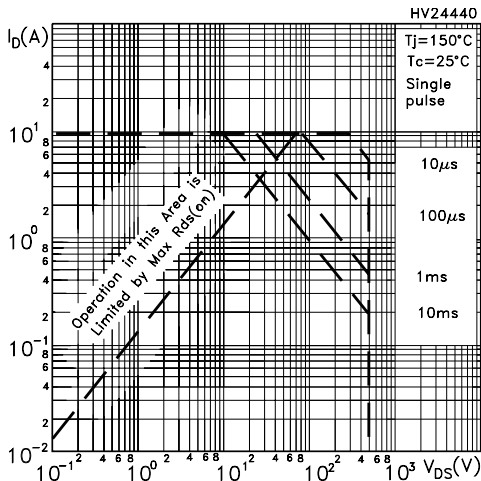


Figure 5: Output Characteristics

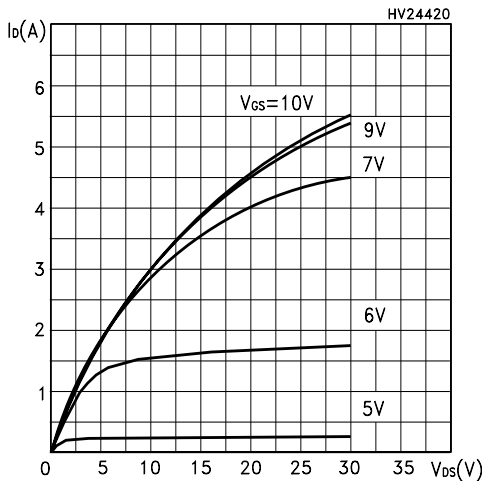


Figure 6: Thermal Impedance TO-92

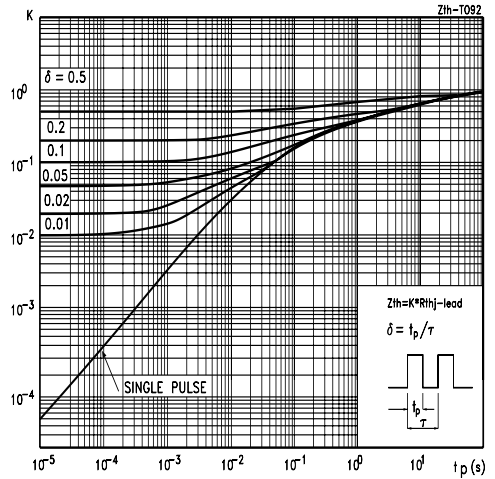


Figure 7: Thermal Impedance For DPAK / IPAK

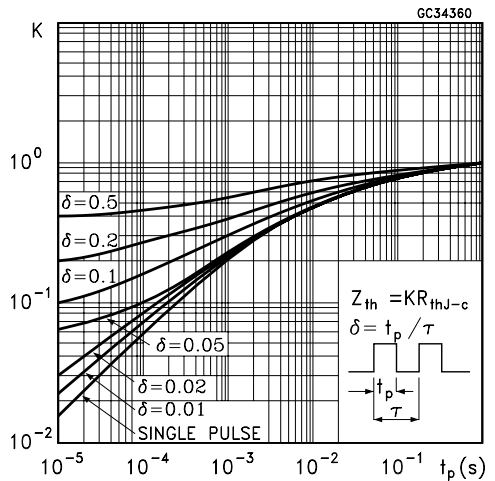


Figure 8: Transfer Characteristics

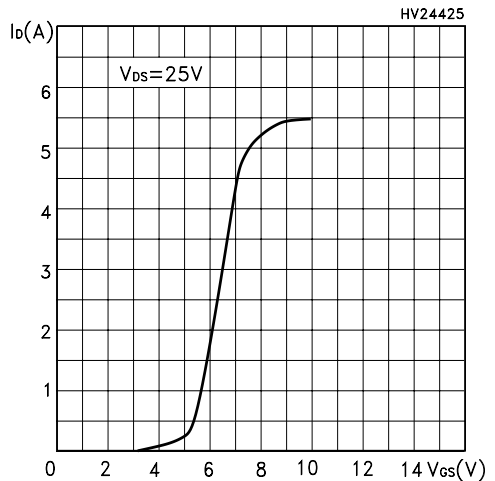


Figure 9: Transconductance

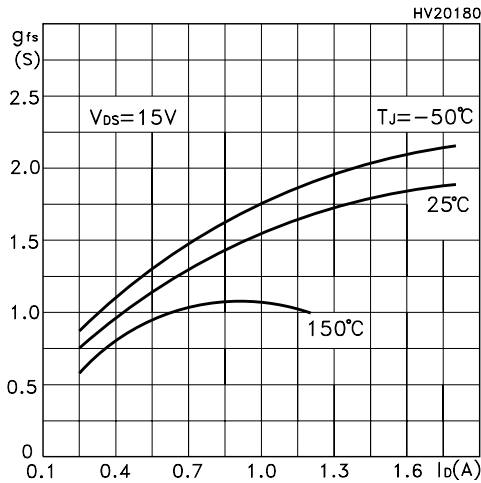


Figure 10: Gate Charge vs Gate-source Voltage

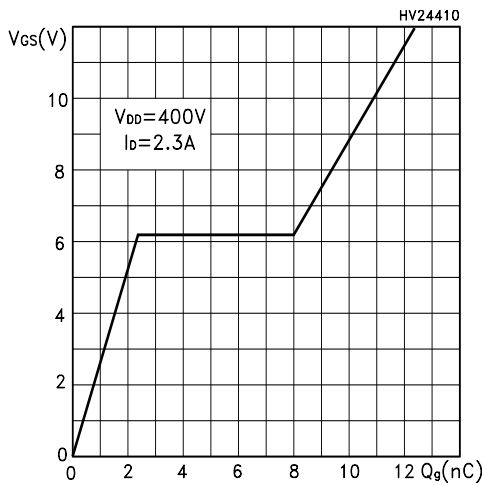


Figure 11: Static Drain-Source On Resistance

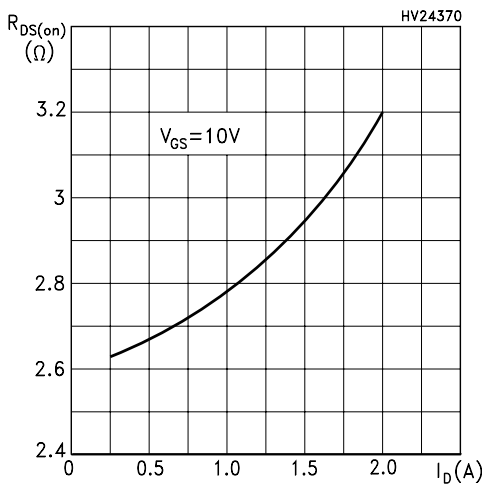


Figure 12: Capacitance Variations

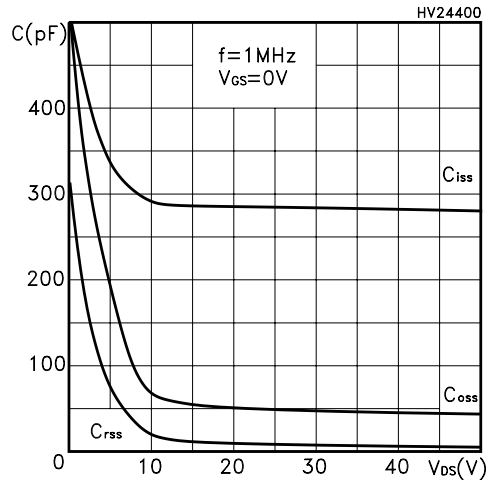


Figure 13: Normalized Gate Threshold Voltage vs Temperature

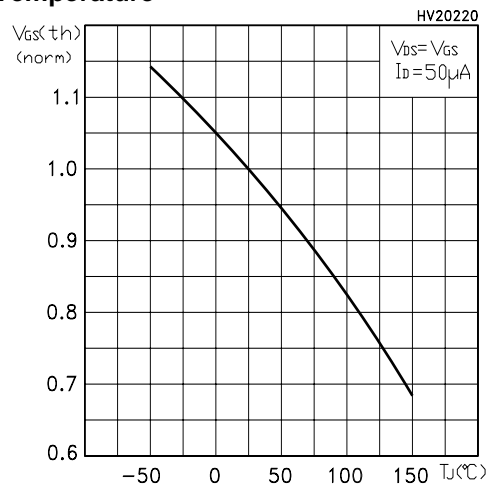


Figure 14: Source-Drain Forward Characteristics

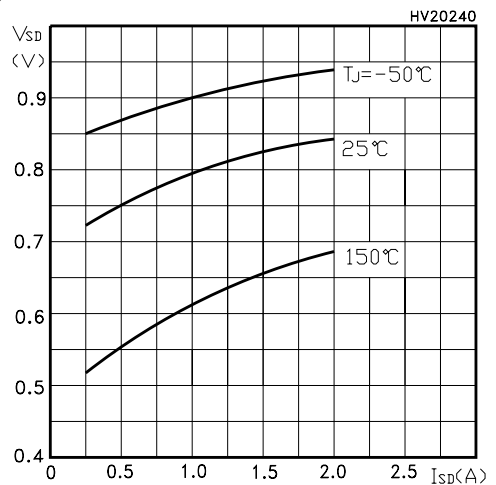


Figure 15: Maximum Avalanche Energy vs Temperature

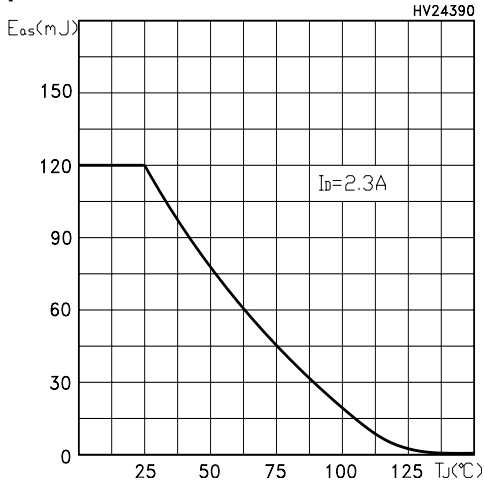


Figure 17: Normalized BV_{DSS} vs Temperature

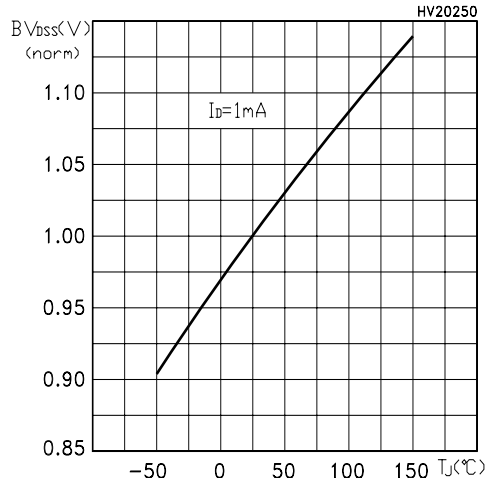


Figure 16: Normalized On Resistance vs Temperature

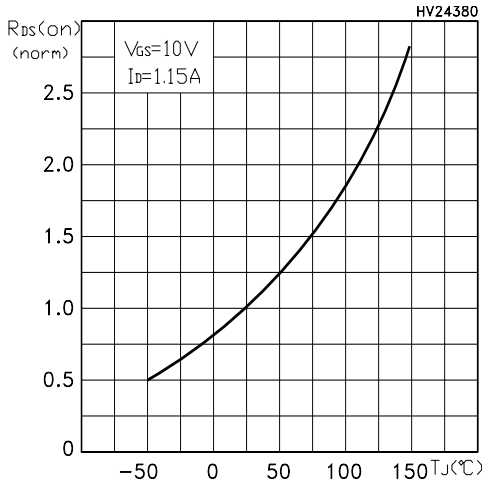


Figure 18: Unclamped Inductive Load Test Circuit



Figure 19: Switching Times Test Circuit For Resistive Load



Figure 20: Test Circuit For Inductive Load Switching and Diode Recovery Times

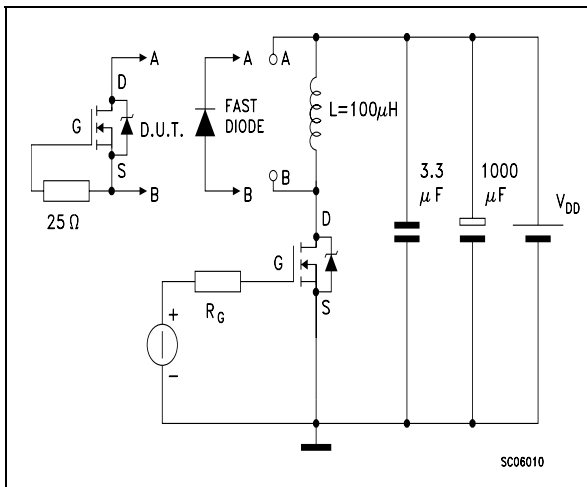


Figure 21: Unclamped Inductive Waferform

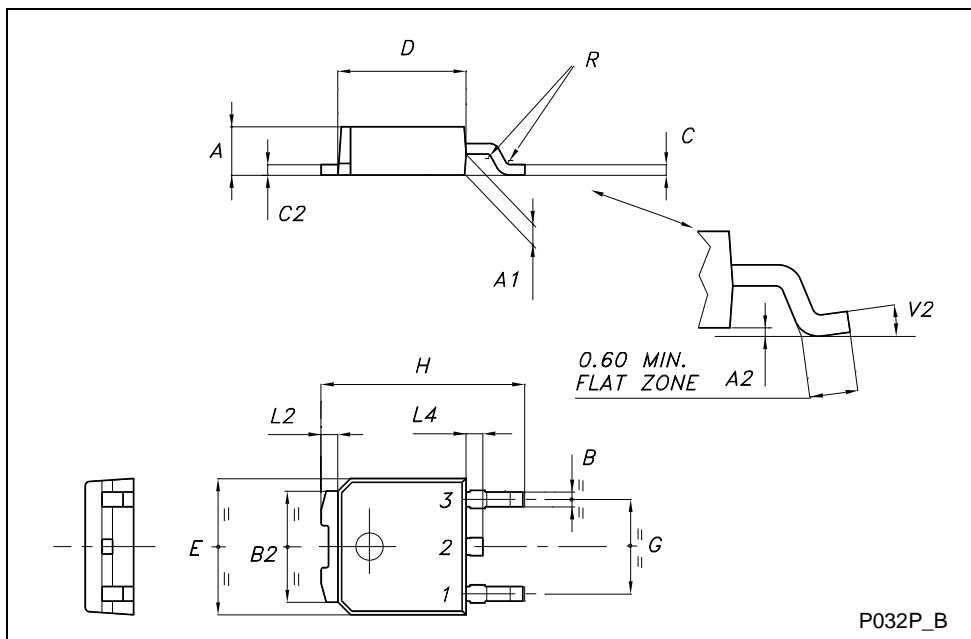


Figure 22: Gate Charge Test Circuit



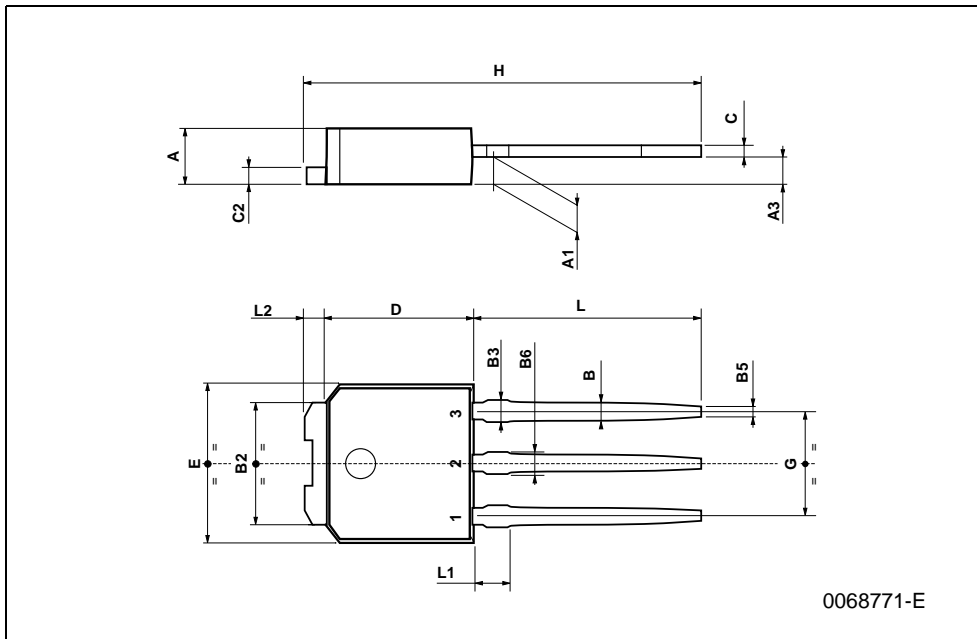
TO-252 (DPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.20		2.40	0.087		0.094
A1	0.90		1.10	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.90	0.025		0.035
B2	5.20		5.40	0.204		0.213
C	0.45		0.60	0.018		0.024
C2	0.48		0.60	0.019		0.024
D	6.00		6.20	0.236		0.244
E	6.40		6.60	0.252		0.260
G	4.40		4.60	0.173		0.181
H	9.35		10.10	0.368		0.398
L2		0.8			0.031	
L4	0.60		1.00	0.024		0.039
V2	0°		8°	0°		0°



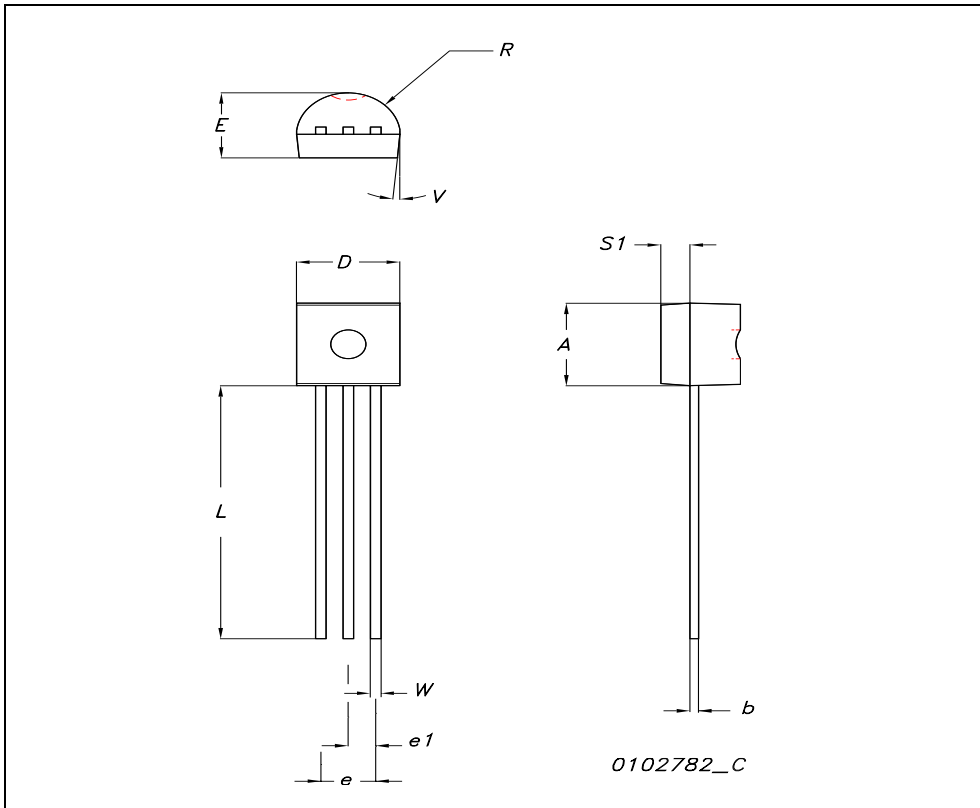
TO-251 (IPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039

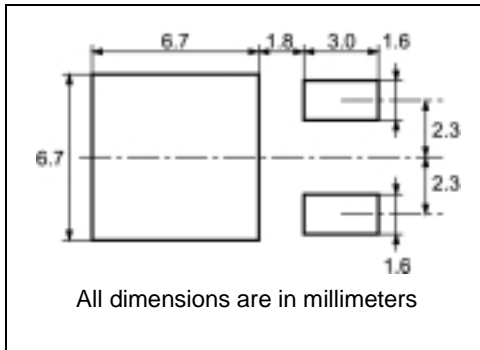


TO-92 MECHANICAL DATA

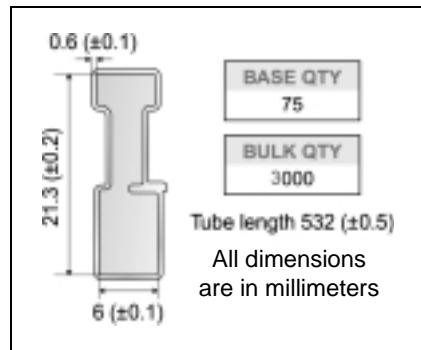
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.32		4.95	0.170		0.194
b	0.36		0.51	0.014		0.020
D	4.45		4.95	0.175		0.194
E	3.30		3.94	0.130		0.155
e	2.41		2.67	0.094		0.105
e1	1.14		1.40	0.044		0.055
L	12.70		15.49	0.50		0.610
R	2.16		2.41	0.085		0.094
S1	0.92		1.52	0.036		0.060
W	0.41		0.56	0.016		0.022
V		5°			5°	



DPAK FOOTPRINT



TUBE SHIPMENT (no suffix)*



TAPE AND REEL SHIPMENT (suffix "T4")*

REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641

* on sales type

TO-92 AMMOPACK

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A1	4.45		4.95	0.170		0.194
T	3.30		3.94	0.130		0.155
T1			1.6			0.06
T2			2.3			0.09
d	0.41		0.56	0.016		0.022
P0	12.5	12.7	12.9	0.49	0.5	0.51
P2	5.65	6.35	7.05	0.22	0.25	0.27
F1, F2	2.44	2.54	2.94	0.09	0.1	0.11
delta H	-2		2	-0.08		0.08
W	17.5	18	19	0.69	0.71	0.74
W0	5.7	6	6.3	0.22	0.23	0.24
W1	8.5	9	9.25	0.33	0.35	0.36
W2			0.5			0.02
H	18.5		20.5	0.72		0.80
H0	15.5	16	16.5	0.61	0.63	0.65
H1			25			0.98
D0	3.8	4	4.2	0.15	0.157	0.16
t			0.9			0.035
L			11			0.43
I1	3			0.11		
delta P	-1		1	-0.04		0.04

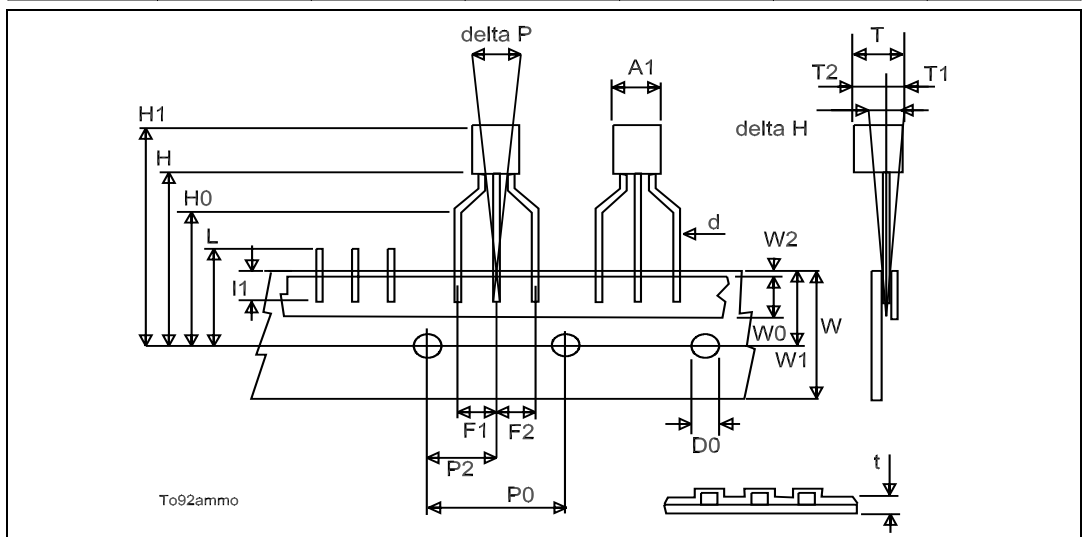


Table 10: Revision History

Date	Revision	Description of Changes
09-Jul-2004	1	First Release.
17-Jan-2005	2	Complete Version

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